Novel backside structure with improved energy resolution.

G. Prigozhin, M. Pivovaroff, S. Kissel, M. Bautz, G. Ricker

Center for Space Research, Massachusetts Institute of Technology,
Cambridge, MA 02139

ABSTRACT

We have experimentally shown that heavily doped p+ layer at the silicon - silicon dioxide interface leads to charge losses in the signal electron clouds due to surface recombination and results in degraded energy resolution of the response of backside illuminated AXAF CCDs to low energy X-rays. The size of secondary ionization cloud generated by an incident X-ray photon can be much larger than that predicted from higher energy electron range-energy relations because of the long range of low energy nearly thermalized electrons. As a result, charge can be lost to recombination at the back surface even for photons interacting thousands of angstroms from the back surface. We propose a new backside illuminated structure which should be able to achieve the same level of energy resolution as the frontside illuminated CCD, while having high quantum efficiency at low energies. It shrinks the area of the heavily doped silicon to less than 2% of the pixel area, thus dramatically reducing recombination losses. If this design is combined with fully depleted silicon structures, it promises a highly efficient X-ray sensor with a good energy resolution throughout the 0.1 - 15 keV band.

Keywords: X-ray, charge coupled devices, energy resoulution, backside illumination

1. INTRODUCTION

Numerous attempts to create a device with high quantum efficiency (QE) at low energies (below 1 keV) and good energy resolution have been so far unsuccessful. While frontside illuminated CCDs can achieve energy resolution close to the theoretical limit, they suffer from a significant absorption of photons in the polysilicon gates and therefore have a poor QE. Backside illuminated CCDs have high QE but their energy resolution is poor due to electron losses at the back surface.

An attempt to increase the QE of frontside illuminated devices by removing polysilicon from the part of the pixel and leaving it open was described in.[1] The surface of the open area of the device was doped with boron to pin the surface potential and thus is no different from the illuminated surface of the backside structure, except that it is located at the front surface. The histogram of the response of the device to monochromatic low energy X-rays exhibits two distinct peaks corresponding to the different portions of the pixel. The peak at higher energy comes from the gate covered area, another one, wide and shifted to lower pulseheights, originates from the open p^+ doped area. This clearly indicates that the degradation of energy resolution in the backside devices is caused not by spreading of the charge cloud during transfer from the back surface to the CCD potential well, but rather by charge losses somewhere in the p^+ layer.

A similar conclusion can be drawn from the results published by the MPI group.[2] The shape of the response and the energy resolution of their backside illuminated devices depends sharply on the treatment of the back surface p^+ layer, again indicating that charge losses in this layer are responsible for the degradation of the peak width.

It is usually overlooked that a regular frontside illuminated CCD has a fraction of its pixel which is somewhat similar to the backside illuminated CCD structure and can be used to gain understanding of the poor performance of the latter. Channel stops are regions where relatively heavily doped p^+ layer is formed near the surface of the high resistivity substrate, the surface being covered by a layer of SiO_2. The distribution of dopant is not the same as in the p^+ implant of the backside device, the thickness of the oxide is much larger, but in general the structure is similar. The main difference between the backside p^+ layer and the channel stop is the polysilicon gate covering the surface of the front side illuminated device. Because the level of doping in channel stop is relatively high, the gate does not have any influence on the conditions inside silicon. It only can change the surface potential, which, as we will see later, can be extremely beneficial for better understanding of the device performance.

Corresponding author: Gregory Prigozhin,e-mail: gyp@space.mit.edu

In this paper we analyze charge losses in the channel stop region and show that under certain conditions charge losses can be entirely suppressed. Based on this new understanding in section 3 we describe a backside illuminated structure which promises good energe resolution comparable to that of the frontside illuminated devices and high QE.

All the experimental work discussed in this paper was performed on the ACIS CCDs manufactured at the MIT Lincoln Laboratory for the Chandra X-ray Observatory. Detailed discussion of these devices can be found in.[3]

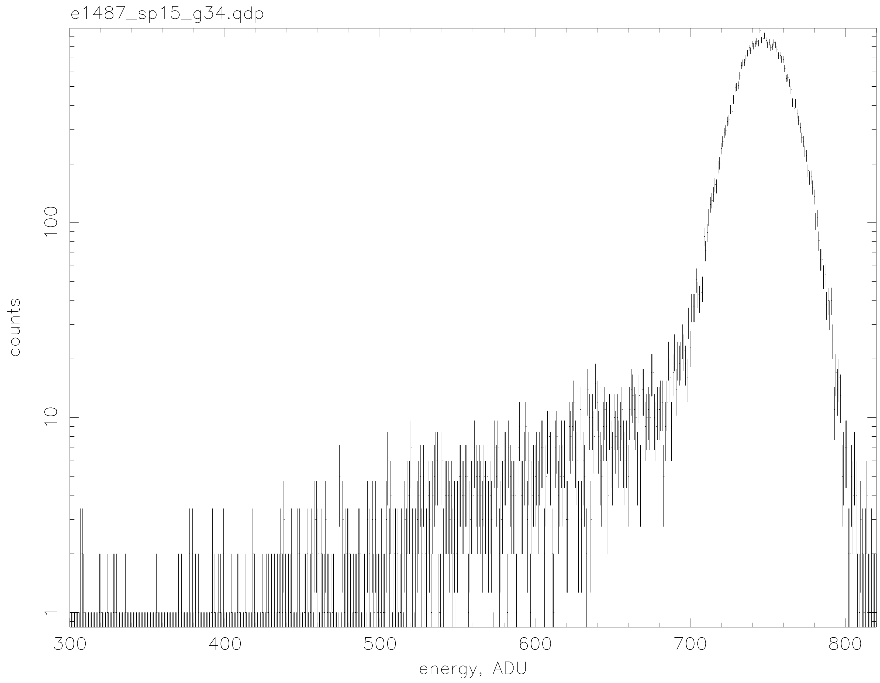

Figure 1. Histogram of the horizontally split events at 1487 eV.

2. MECHANISM OF CHARGE LOSSES IN THE CHANNEL STOP REGION

We have recently experimentally proved [4] a long standing suspicion that that all horizontally split events (an event that has signal charge in two adjacent pixels in the same row) are coming from the region underneath the channel stops where the charge clouds split between two adjacent pixels. This was one of the numerous results produced by the so-called mesh technique which allows to observe the event distribution inside one pixel of a CCD.

It means that analysis of the distribution of the horizontally split events, by itself an important part of the model of the fronside illuminated CCD response, can also be an important tool in studying of the charge cloud dynamics in the p^+ region of the channel stop. Due to the similarity of this layer to the p^+ layer of the backside structure this can provide insight into the mechanism of the charge loss in a backside illuminated device.

A typical example of the histogram of the horizontally split events is shown on Fig. 1 for the monochromatic 1487 eV X-ray source. Next to the main peak it has a distinct low energy shoulder. It was shown in[6,7] that the shoulder events originate from the charge clouds formed inside p^+ region and suffering charge losses. The shape of the shoulder depends on the energy of the incoming photons. The relative strength of the shoulder grows at lower photon energies as the penetration depth of the photons diminishes and the fraction of photons interacting near the surface goes up.

In order to determine where in a pixel are shoulder events formed we utilized the power of the mesh technique.[4,5] An idea of this technique is to place an opaque metal foil with an array of tiny square holes (1.4 × 1.4 microns in our case) on the surface of the CCD. The pitch of the holes is the same as the pitch of the CCD pixels, but due to a small rotation angle between the mesh array and CCD, each hole sees slightly different portion of the pixel. A CCD is then illuminated by soft X-rays which are stopped by the foil. A proper analysis of the data under assumption that all the pixels are identical produces a distribution of the X-ray intensity inside one pixel.

In our experiments a CCD was illuminated with monochromatic 525 eV X-rays (oxygen emission K line) with a mesh applied to the surface of the device. At this energy X-ray penetration depth in silicon is only 0.5 microns and very significant fraction of the photons hitting channel stop region is stopped inside p^+ region, making amplitude of the shoulder in horizontally split events at least as big as the main peak amplitude.

All the detected events were separated according to their amplitude in two groups: "shoulder events" and "photo-peak events". Upper plot on Fig. 2 shows a summary histogram and the boundaries that define the two groups. Two lower diagrams at Fig. 2 show a spatial distribution inside a pixel of the sum of the ASCA grade 3, 4, and 6

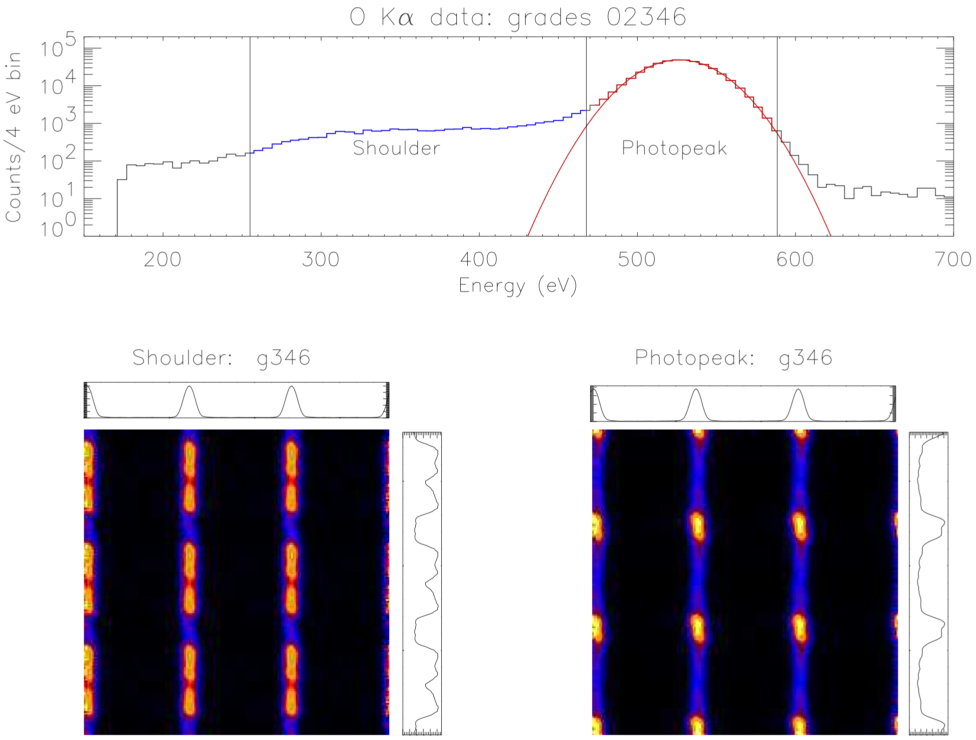

Figure 2. Histogram of combined grades 0, 2, 3, 4, 6 showing limits for "main peak events" and "shoulder event" (upper plot); intra-pixel distribution of the "shoulder events" (lower left) and the "main peak events" (lower right).

events (grades 3 and 4 are horizontally split events, grade 6 is 3- and 4-pixel events formed near the pixel corner). As expected, all the shoulder events are formed in the channel stop region, indicating that the charge losses indeed occur somewhere inside p^+ region. What was entirely unexpected, there are almost no shoulder events under one of the gates.

In this measurement one of the three gates of the CCD pixel was held at a low voltage of -5 Volts, separating potential wells formed under two other gates with a high level voltage of +5 Volts. The mesh technique allows to identify each gate, and it is a low voltage gate where intensity of shoulder events drops down to zero. The histogram of the events under the low voltage gate looks similar to the histogram of the events in the pixel center containing only main peak and does not have a low energy shoulder. This means that charge clouds under this gate do not suffer charge loss, even if they are formed in the p^+ region.

The explanation of the charge loss suppression becomes clear if the potential distribution near the surface of silicon is considered. Positive gate voltage creates a potential well for electrons at the surface. Since silicon is heavily doped in that region and the oxide layer is thick, the penetration depth of the electric field is very small. Still, this structure is an equivalent of a surface channel CCD which collects some signal charge from the p^+ region where there is almost no electric field and charge diffuses in all directions. Once electrons reach the $Si - SiO_2$ interface, they have a high probability to get trapped and recombine at the surface. Meanwhile, negative gate voltage repels signal electrons away from the surface, thus preventing surface recombination losses. In this case signal charge is reflected away from the surface and gets collected into the CCD potential wells.

The consequence of this discovery is that the charge loss in the doped p^+ region is entirely due to surface recombination and can be eliminated if the structure has a gate which can drive the surface into the hole accumulation mode.

It is clear that at some gate voltage between +5 and -5 Volts a transition should occur from the high level of charge loss in the channel stop region to a very low level of charge loss. A next logical step was to scan through the range of voltages applied to the gate to find out when does this transition happen.

While the mesh technique provides the most detailed information about the distribution of amplitudes inside the pixel, it requires very long data acquisition runs and very complicated and laborious analysis. Because of that we chose to illuminate device uniformly with monochromatic X-rays and look at the shape of the horizontally split events as a measure of the charge losses in the channel stop region.

At photon energy 525 eV, right below oxygen absorption edge, sufficient amount of photons penetrate through SiO_2 layer to produce a noticeable peak in the horizontally split events. Penetration depth in silicon at this energy is only 0.5 microns, and most of the photons interact very close to the surface. As a consequence, the shape of the peak in a histogram depends sharply on the degree of surface charge loss. Figure 3 shows a rapid change of the histogram shape as the voltage V_g at the two integrating gates is increased from +0.25 to +2.75 Volts. At 0.25 Volts the primary peak is narrow and has pretty much gaussian shape, its width (57 eV) not much larger than 46 eV FWHM of the single pixel event peak. As the voltage increases, the peak broadens significantly and then there appears the second

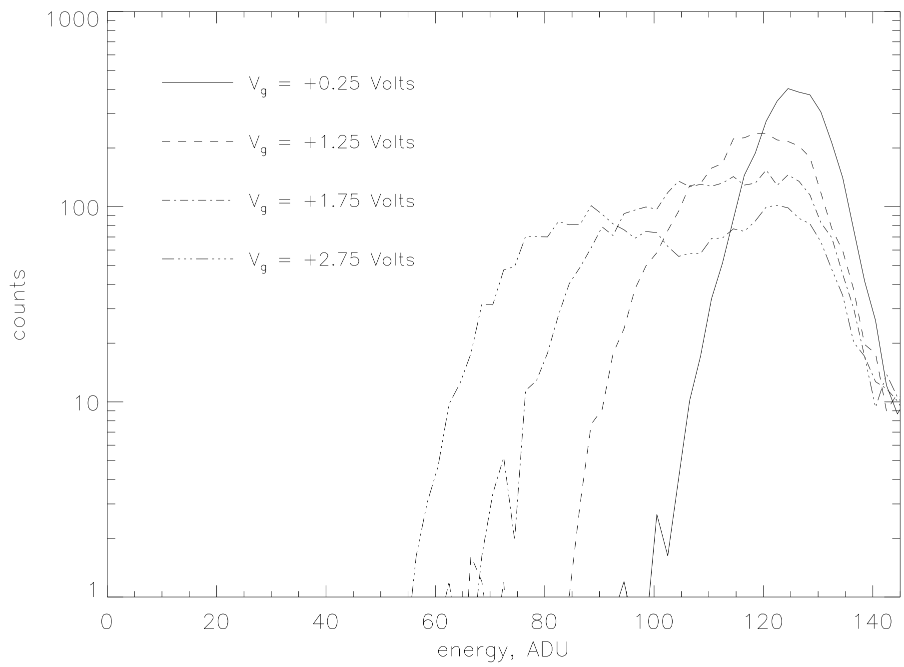

Figure 3. Histograms of the horizontally spit events at different gate voltages. Two gates were held high during the data acquisition. The low gate voltage was maintained 5 Volts lower than at two other gates. Incident photon energy 525 eV.

low energy peak formed by the electron clouds which lost significant fraction of charge to the surface recombination centers. Gradual broadening is an indication that amount of charge lost by each electron cloud is increasing with gate voltage, not only the number of such clouds goes up. The number of "lossy events" reach saturation at 2.75 Volts and does not grow further as the gate voltage goes up. The reason for the saturation is that for every electron cloud formed inside the p^+ layer where electric field is nearly absent some fraction of charge will reach the surface and will get lost. The change in surface potential can change the fraction of lost elctrons in each particular cloud, but it does not change the depth of the p^+ layer. Thus, the relative intensity of the low energy shoulder can be used to measure the depth of the p^+ layer. The result of such measurement [5] (0.35 microns) is in a very good agreement with the results of the simulation of the electric field distribution in CCD.

The ability of the gate with negative voltage to repel electrons away from the surface in some sense agrees well with what we discovered earlier[8]: for single pixel events (they are formed in the central part of the pixel) originating from the photons interacting near silicon surface the cloud size is almost an order of magnitude smaller compared to the clouds formed deep in the bulk of silicon. The reason is similar - in the buried channel CCD the electric field near the surface repels low energy nearly thermalized electrons preventing them from reaching the surface, thus reducing the number of clouds which suffer charge loss.

3. A CONCEPT OF A BACKSIDE DEVICE

The results described above suggest that the same mechanism of the charge loss is responsible for the broadening of the main peak of the response of the backside illuminated devices. In fact, the shape of the response of the backside devices is very similar to the curve on Fig. 3 corresponding to the gate voltage of +1.25 Volts.

The results described above suggest a solution which is likely to significantly improve energy resolution of the backside illuminated devices. It is clear that the charge clouds formed near the back surface of the backside illuminated device suffer the same type of charge losses to the surface recombination centers as the clouds near the surface of the channel stop. This explains the poor energy resolution of the backside devices, similar to that of the channel stop region at positive gate voltages. In fact, the shape of the response of the backside devices is very similar to the curve on Fig. 3 corresponding to the gate voltage of +1.25 Volts. Backside device resolution is also worsened by the weak electric field near the illuminated surface and bad charge transfer efficiency, but the main factor is surface recombination.

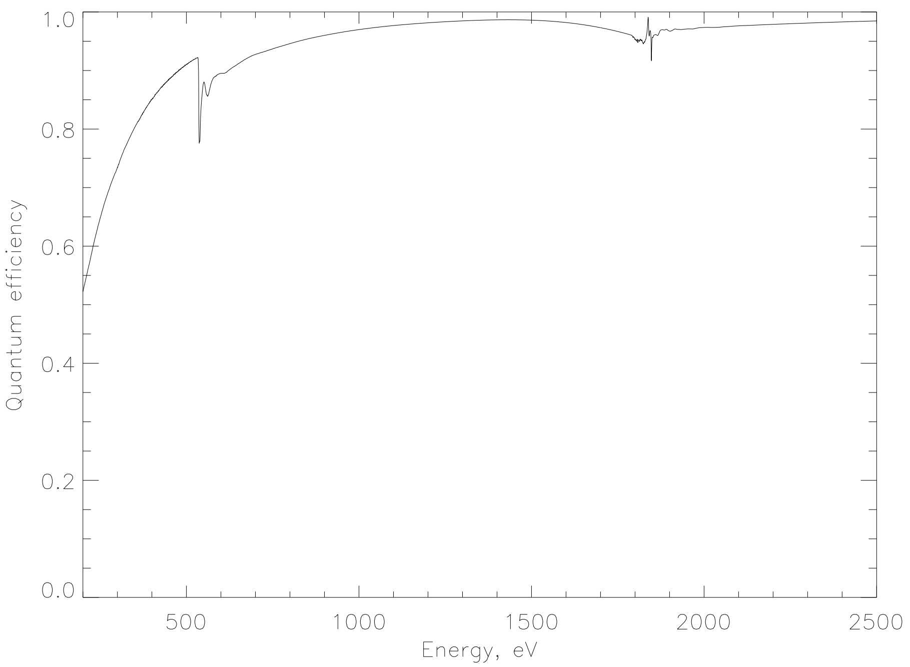

Figure 4. Quantum efficiency of the proposed device as a function energy. The device is covered by 30 nm of SiO_2 and 25 nm of polysilicon.

Normally the surface of the backside illuminated device is covered by a thin layer of SiO_2. If the oxide is covered by a conductive gate, it would allow a bias to be applied to the gate to drive the surface into hole accumulation mode, suppressing surface recombination. Such a gate does not have to carry any current. Thus, it can be made very thin, its high resistivity will not pose a problem.

In the channel stop region even very small negative voltage at the gate is sufficient to suppress surface recombination. This means that a very small voltage is necessary to control the gate of the MOS capacitor on the back surface, and the electric field in the oxide does not need to be higher than in the oxide above channel stop region.

An addition of the gate to the structure will, of course, reduce the quantum efficiency of the device. But if the layer is very thin, the QE will still be sufficiently high at low energies. On Fig. 4 is shown calculated QE as a function of energy, assuming that structure is covered by a polysilicon gate 25 nm thick, SiO_2 layer thickness is 30 nm. The most simple structure for test purposes would be a regular backside illuminated device covered by a thin polysilicon gate. Once the entire surface of the device is covered by the gate, there is no need for an uninterrupted p^+ layer at the back. This layer serves as the drain for the holes and is needed to pin the potential of the back surface. But now that the gate can hold the potential steady, p^+ region can be reduced to just narrow strips, which is enough for the purpose of draining holes. Fig. 5 shows the cross-section of such device with the reduced p^+ area. Smaller area of the

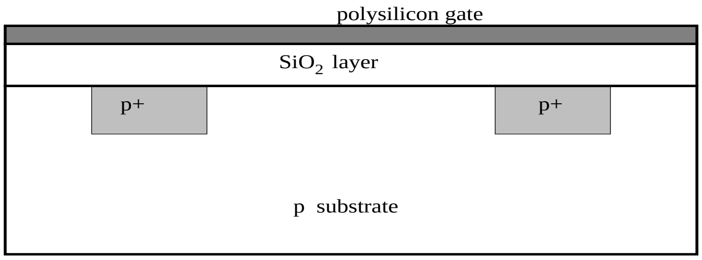

Figure 5. Cross section of the suggested device structure with the reduced area of p^+ dopant at the back surface.

doped silicon is likely to reduce stress and the amount of damage near the back surface, thus further reducing surface recombination. It can also cause charge focusing effect if p^+ strips on the back surface are aligned with the fronside channel stops. This structure would need a photolithography made on the back surface of the device; alignment requirements, though, are not critical at all. Such a structure looks most attractive as a part of the fully depleted device (throughout the entire wafer), similar to the $p-n$ CCDs [2] or fully depleted CCDs .[9] It could then combine large QE at both high- and low-energy parts of the spectrum with decent energy resolution.

REFERENCES

1. A. Holland, "X-ray spectroscopy using MOS CCDs", Nuclear Instruments and Methods in Physics Research, A 337, 1996, pp. 334-339.
2. R. Hartmann, D. Hauff, P. Lechner, R. Richter, L. Struder, J. Kemmer, S. Krisch, F. Scholze, G. Ulm, "Low energy response of silicon pn-junction detector", Nuclear Instruments and Methods in Physics Research, A 377, 1996, pp. 191-196.
3. B.Burke, J.Gregory, M.Bautz, G.Prigozhin, S.Kissel, B.Kosicki, A.Loomis, D.Young, "Soft-X-Ray CCD Imagers for AXAF", IEEE Transactions on Electron Devices, vol.44, No.10, pp. 1633-1642, October, 1997.
4. M. Pivovaroff, S. Jones, M. Bautz, S. Kissel, G. Prigozhin, G. Ricker, H. Tsunemi, E. Miyata, "Measurement of the subpixel structure of AXAF CCD's", IEEE Transactions on Nuclear Science, v. 45, No. 2, 1998
5. M. Pivovaroff, S. Kissel, G. Prigozhin, M. Bautz, G. Ricker, "In-situ measurement of the channel stop structure in AXAF CCDs", These Proceedings.
6. G. Prigozhin, "X-ray detection in channel stops", MIT ACIS memo # 150, 1998, (http://space.mit.edu/˜gyp/memos.html).
7. G. Prigozhin, A. Rasmussen, M. Bautz, G. Ricker, "A model of the X-ray response of the ACIS CCD", SPIE Proceedings, vol. 3444, pp. 267-275, July, 1998.
8. G. Prigozhin, S. Jones, M. Bautz, G. Ricker, "Physics of the low energy tail in the ACIS CCD. Spectral redistribution function", Nuclear Instruments and Methods in Physics Research, A, 1999 *in press*.
9. S. Holland, D. E. Groom, M. E. Levi, N. P. Palaio, S. Perlmutter, R. J. Stover, and M. Wei, "Large Format CCD Image Sensors Fabricated on High Resistivity Silicon," Proc. 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 10-12, Karuizawa, Nagano, Japan, pp 179-182.