1.9 Effects of Instrument Configuration and Environment on Detector Calibration

1.9.1 Effects of Parallel Register Clock Levels on Detection Efficiency

The clock voltages in the image section of a CCD determine the depletion depth of the device. The more positive both levels (low and high) are, the bigger is the depletion depth and, hence, the high energy quantum efficiency. For this reason the standard levels were chosen to be as high as they can safely be, namely, +11 Volts being the high level and +2 Volt the low level. An attempt to further increase the high level voltage above +12 Volts resulted in an increased dark current due to avalanche multiplication of electrons in the channel (so-called "spurious charge" effect). In order to reduce dark current in the frame store section the low clock level there is set to -4.5 Volts. This keeps the surface of silicon under nonintegrating gates in inverted mode, thus suppressing surface generation centers. With the standard levels (+2,+11 Volts) in the image section the depletion depth of the devices varies around a typical value of 70 microns.

For each of the flight devices a measurement was also made with reduced clock levels in the image section. The voltges were chosen to keep nonintegrating gates in inversion with the clock levels at -4.5 and +5 Volts. During calibration the devices did not show any difference in the dark current for the two modes. But the reduced level mode may prove useful when a device undergoes irradiation in space and the level of dark current goes up. The drawback of reducing image clock levels is a reduced depletion depth and, consequently, reduced quantum efficiency at energies above 4 keV. The depletion depth of each flight device was measured in both modes, and results can be found in the Table 1.30 of Section 1.6.2.

In Fig. 1.96 is shown a calculated ratio of quantum efficiencies for the device w193c2 in two different modes. The measured depletion depths for the two modes were found to be 65 and 48 microns, respectively, for standard and reduced voltages. Based on these numbers quantum efficiency was calculated for each mode.

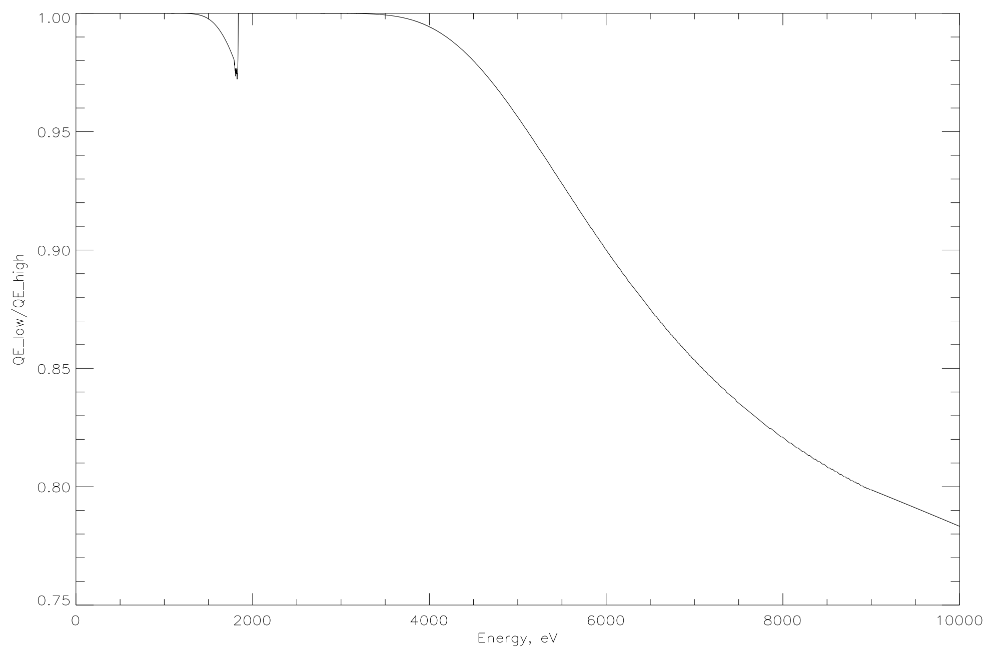

Figure 1.96: The ratio of quantum efficiencies for the device w193c2 with the standard clock levels and the reduced clock levels.

1.9.2 Effects of Focal Plane and Detector Electronics Temperature

1.9.2.1 Detector Electronics Temperature

Prior to delivery to XRCF, the ACIS integrated flight instrument underwent testing at MIT Lincoln Laboratories. Some of these measurements involved operating ACIS with the Detector Electronics Assembly (DEA) at temperatures of -17 C° and 20 C°. These tests were used to map the gain dependence on the electronics temperature. A detailed description and analysis of the gain calibrations are reported in ACIS Memo #143 [19]. The main points are summarized below:

–The DEA was stabilized at temperature T_i, (T_i = -17 C°, 20 C°)
–Each chip was independently illuminated with an Al Kα source and an ^{55}Fe source
–The focal plane (FP) temperature during these measurements ranged between $^-$116–$^-$119 C°
–Gains were calculated by fitting a linear relationship to a gaussian centroid for the Al Kα and the Mn Kα line

Table 1.65 lists the mean gain for each chip for DEA temperatures of 20 C° (hereafter $LLTV_{hot}$) and -17 C° (hereafter $LLTV_{cold}$). Table 1.65 also lists the average chip gains calculated from the XRCF Flat Field ($XRCF_{FF}$), Phase I data. See Section 1.3.1 for the details of these measurements.

It is clear from the data that the gains increase with increasing DEA temperature. In order to quantify this relationship, we have made a linear fit of the gains as a function of temperature. Figure 1.97 shows the linear best-fit plotted against the measured gain values. The hash marks simply indicate the data point and are not representative of errors. The LLTV$_{cold}$ data for I0 and S0 are known to have a problem with drifting biases, so these two data points are suspect[7]. With only three data points to fit, the incorrect LLTV$_{cold}$ gains greatly influence the fits and skew the slope of the expected lines. Excluding I0 and S0, the data seem to follow the linear relationship quite reasonably. The small deviations from linearity are expected, as only two data were used to define the LLTV gains.

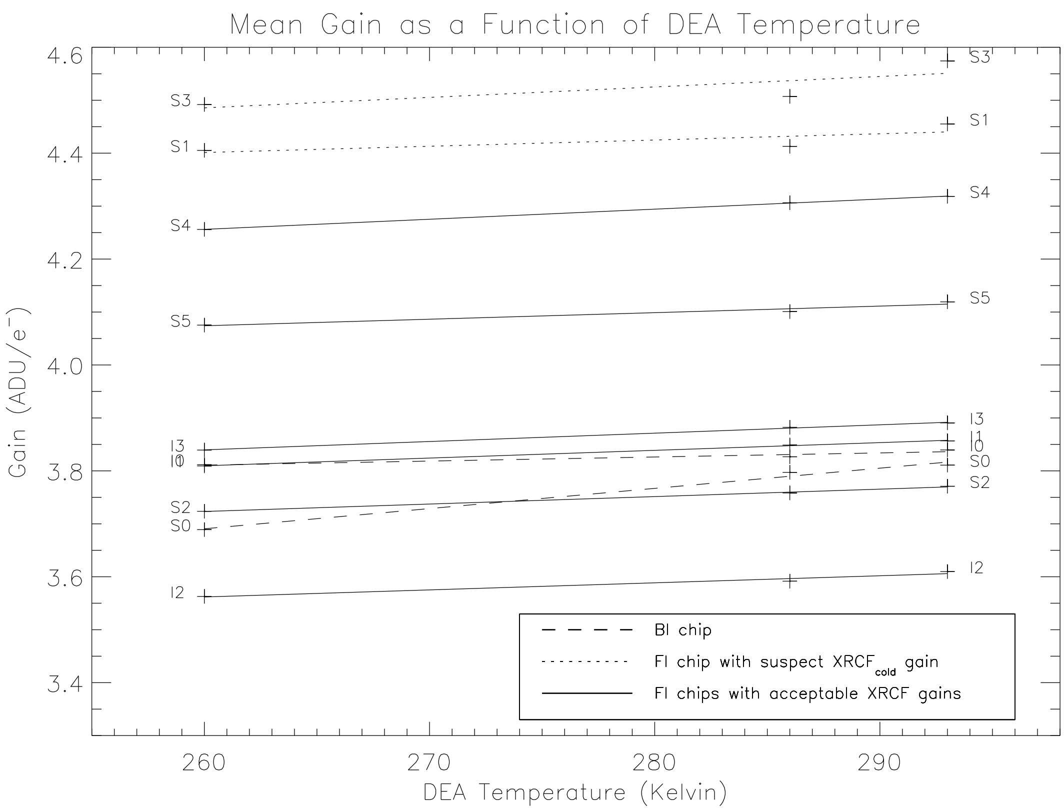

Figure 1.97: ACIS gain variation as a function of DEA temperature.

[7]This problem is fully characterized in ACIS Memo #143. The jitter.dacs software patch implemented during the XRCF Flat Field measurements eliminates this problem.

1.9.2.2 Focal Plane Temperature

In addition to being affected by the temperature of the readout electronics, the gain is also dependent on the temperature of the focal plane (FP). Part of the the MIT CSR sub-assembly calibration efforts included operating each flight chip at off-nominal temperatures to study the influence of this effect on gain. Table 1.66 lists the mean gains and gain variation dependence on chip temperature, as calculated at MIT CSR . Each chip was operated at $^{-}110$ C$^\circ$, $^{-}120$ C$^\circ$ and $^{-}130$ C$^\circ$ and illuminated with an ^{55}Fe source. Gains were determined by fitting a gaussian to the Mn Kα line and assuming an identically linear (i.e. no offset) relationship between the centroid and 5.895 keV. The differences between the MIT CSR mean gains and the LLTV/XRCF mean gains (Table 1.65) result from not using the flight electronics at MIT CSR.

Before calculating the gain dependence on DEA temperature, we must account for the fact that the FP was operated at slightly different temperatures during the LLTV and XRCF calibrations. Using the (dln(G)/dT$_{chip}$) calculated from the MIT measurements, the expected increase in gains from operating the FP at $<^{-}117.5>$ C$^\circ$ instead of $^{-}110$ C$^\circ$ is on order of 0.002 ADU/eV. This amount has no affect on the derivation of the gain dependence on DEA temperature. For comparison, .002 ADU/eV corresponds to roughly twice the thickness of a line in in Figure 1.97. If we neglect the very small effect caused by different FP operating temperatures, the DEA temperature dependent variations are determined by the linear fit term divided by the mean gain. These values are also listed in Table 1.66

FP Location	Mean Gain (eV/ADU) LLTV$_{cold}$ DEA=$^{-}$17 C° FP=<$^{-}$117.5> C°	XRCF$_{FF}$ DEA=13 C° FP=$^{-}$110 C°	LLTV$_{hot}$ DEA=20 C° FP=<$^{-}$117.5>
I0	3.812	3.827	3.840
I1	3.809	3.849	3.857
I2	3.563	3.592	3.610
I3	3.839	3.882	3.891
S0	3.689	3.797	3.811
S1(BI)	4.405	4.413	4.455
S2	3.724	3.758	3.771
S3(BI)	4.492	4.507	4.574
S4	4.256	4.306	4.319
S5	4.075	4.101	4.119

Table 1.65: Mean gains for ACIS at different operating temperatures

	MIT CSR		**LLTV/XRCF**
FP Location	Mean Gain at chip=$^{-}$120 C° (eV/ADU) (HIREFS)	Gain Temp Variation (dln(G)/dT$_{chip}$) x10^{-5} (C^{-1})	Gain Temp Variation (dln(G)/dT$_{DEA}$) x10^{-4} (C^{-1})
I0	3.990	< 6	2.0
I1	3.972	< 6	3.8
I2	3.865	-10	3.7
I3	4.250	< 6	4.1
S0	4.059	54	10
S1(BI)	5.134	< 6	2.7
S2	4.042	< 6	3.7
S3(BI)	5.109	< 6	4.4
S4	4.375	-8	4.4
S5	4.316	< 6	3.0
mean			**4.2**

Table 1.66: Gain dependence on chip temperature and DEA temperature

1.9.3 Long Term Gain Stability

Checking the long term gain stability of the ACIS chips is an important step in the pre-launch calibration. During the course of sub-assembly calibration, the stability in chip gain was firmly established and it is completely expected that ACIS CCD's will share this characteristic. While the earliest gain measurements of the flight instrument date back to March 1997 (LLTV), the first high accuracy (i.e. several characteristic Kα lines used) determination occurred at the XRCF Flat Field (XRCF-FF) calibration in May 1997. The next opportunity to measure the gain came during the first thermal vacuum test at Ball (ISIM-TV1) in October 1997. During this test a significant amount of data was acquired from the External Calibration Source (ExtCalSrc), allowing an accurate gain determination of all ACIS chips. Below, we compare the results of these two calibrations.

Table 1.67 lists the mean gains (all four quadrants of a chip) measured at XRCF-FF and ISIM-TV1. Taking the XRCF-FF values as a baseline, the I-Array chips (imaging CCD's and S2 and S3) have higher gains at ISIM-TV1, while the outer S-Array chips (S0,S1,S4,S5) have approximately the same gains. The gain is known to be dependent on DEA temperature and focal plane temperature. As the effect of the focal plane temperature on the gain is an order of magnitude smaller than that of the electronics temperature, we will focus on the later as a possible explanation of the difference in gains between the two measurements. The mean temperature dependence relationship is: d(ln Gain)/dT=4 $\times 10^{-4}$ (see Section 1.9.2 for details). The thermal conditions for both calibrations were nominally the same: focal plane temperature of -110° C, and DEA -Z plane temperature of +13° C. Allowing for a drift in the DEA temperature of $\sim$ 1° C , we would expect a gain variation on order $\sim$ 0.002, much higher than that observed for the I-array chips. Figure 1.98 plots d(ln Gain) for each quadrant of all ten chips.

Chip	XRCF-FF	ISIM-TV1	Chip	XRCF-FF	ISIM-TV1
i0	3.827	3.857	s1	4.413	4.398
i1	3.849	3.892	s2	3.757	3.795
i2	3.592	3.632	s3	4.507	4.560
i3	3.882	3.911	s4	4.306	4.308
s0	3.797	3.791	s5	4.101	4.095

Table 1.67: Mean Chip Gain determined at XRCF-FF and ISIM-TV1

Systematic variations, order of a few degrees, are expected in the DEA temperature; the dashed lines indicate the values of d(ln Gain) expected for ΔT=$\pm$5° C. The outer S-Array chips are mostly distributed between this range, indicating that the gains measured with the ExtCalSrc for these chips are stable, within systematic uncertainties. Another dashed line indicates the value of d(ln Gain) for $\Delta T=25°$ C; the I-Array chips measured with the ExtCalSrc are tightly grouped abou this line. At this time, the source of the gain shift is not known. However, given the uncertainties in the operating conditions and the thermal environment during the ISIM-TV tests, there exists the distinct possibility that a strong thermal gradient existed inside the DEA unit. This condition can explain the apparantly paradoxical behavior that some of the gains indicate that the DEA -Z plane was in fact $\sim 13°$ C, while the other chips indicate that the the electronics were $\sim 25°$ C hotter. This scenario requires that the boards used to read the I-Array chips were in the hottest part of the gradient and furthest from the DEA -Z plane temperature sensor. Further evidence for this hypothesis comes from Internal Calibration Monitor (ICM) data. The ICM can also be used to determine gains, but only for four quadrants. The ICM data was also taken as part of the XRCF-FF tests, as well as during the second ISIM thermal vacuum test, ISIM-TV2[8]. The XRCF-ICM gains (blue symbols in the plot) are also distributed near the $\pm 5°$ C lines, establishing that the ICM source can provide an accurate gain measurement. During ISIM-TV2, however, the ICM gains (orange symbols in the plot) are also grouped about the 25° C line. The fact that the two ISIM thermal vacuum tests were separated by *more than two months* indicates that whatever condition caused the shift in the ExtCalSrc gains was also present during the subsequent testing. If the mechanism was in fact a thermal gradient, it must have have been stable.

[8] ICM data also exists from the AXAF thermal vacuum tests. While the gains are linear and valid, the thermal conditions during data acquisition are relatively unknown, preventing the inclusion of these points in the current analysis.

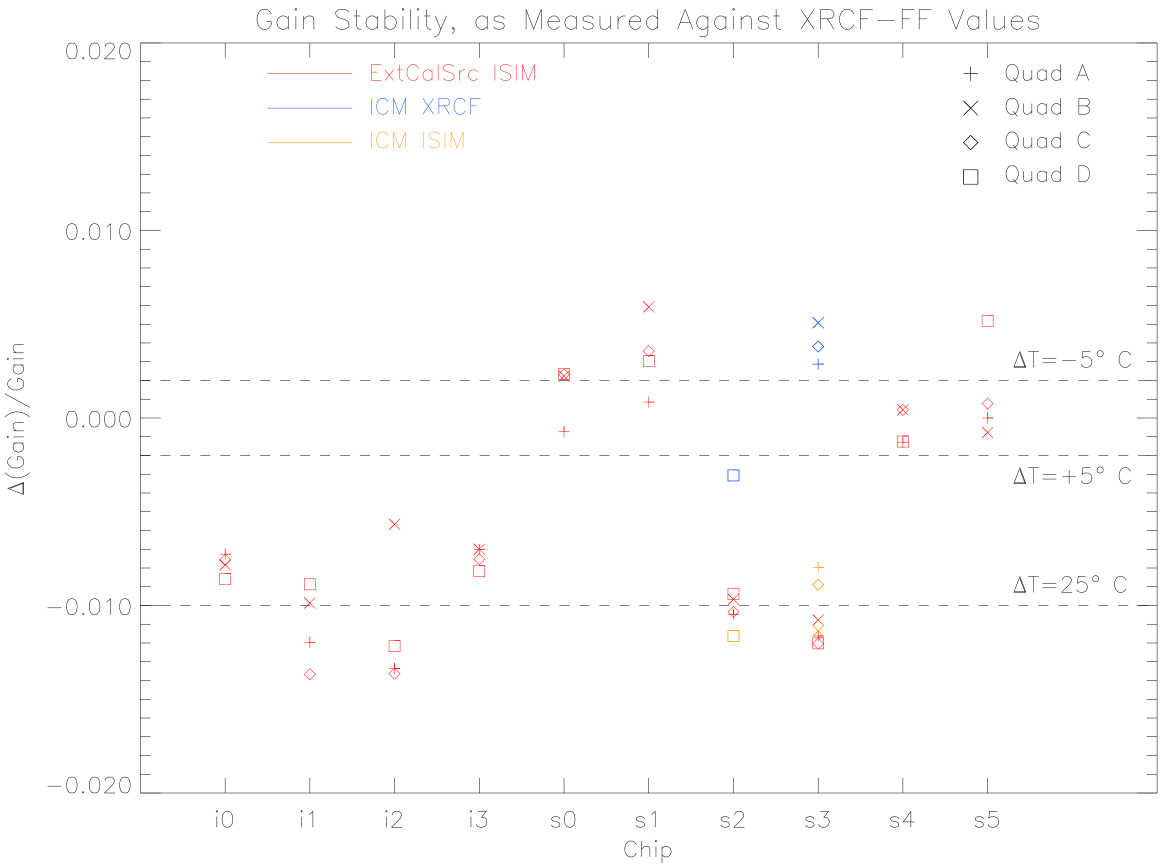

Figure 1.98: The difference in gain measured at XRCF-FF and ISIM-TV1. The figure plots d(ln Gain)=ΔGain/Gain, where the gain from XRCF-FF is taken as a base line.
The red points compare the gains calculated from the ExtCalSrc data at ISIM-TV1, the blue points compare the gains calculated from the ICM source at XRCF-FF, and the orange points compare the gains calculated from the ICM source at ISIM-TV2. The dashed lines and labels indicate the change in DEA temperature required to shift the gain by that amount. The ICM source only allows gain measurements for S2 Quad D and S3 Quads A-C.

1.9.4 Temperature Dependence on Dark Current

1.9.4.1 Introduction

We report on the ACIS dark current measurements made at Ball in October, 1997 as part of the Integrated Science Instrument Module thermal vacuum tests (ISIM-TV1). Below, we describe the procedure used in calculating the dark current and the dark current values for all ten CCDs at temperatures of -40°, -60° and -90° Celsius. We also discuss the measurements made at -90° C used to check the instrument after a thermal cold soak.

1.9.4.2 Procedure

Measurement of dark current requires bias data to be taken using at least two different integration times. During the ISIM TV tests, integration times of 3.3 (short) and 9.9 (long) seconds were used. For each chip eleven frames of data were acquired with the high speed tap (HST) at both the short and long integration times. An average bias frame is created from each set of eleven frames using the `meanbiasclip2` algorithm (/usr/acis/bin/meanbiasclip2). Each of these average bias frames is overclock (OC) corrected before the short average frame is subtracted from the long average frame on a pixel to pixel basis. Specifically, the distribution of differences D is given by

$$D = \sum_{quad=1}^{4} \sum_{col=1}^{256} \sum_{row=1}^{1024} (Pixel(col,row)_{9.9\,sec} - OC(quad)_{9.9\,sec}) \\ -(Pixel(col,row)_{3.3\,sec} - OC(quad)_{3.3\,sec}).$$

A gaussian function is fit to the distribution D, and the dark current is taken as the center of the gaussian divided by the difference in integration times (6.6 seconds). This procedure was repeated for each chip. Data for chips I0, I1, I2, and I3 were taken with ACIS operating in the I-array configuration. Data for chips S0, S1, S2, S3, S4 and S5 were taken with ACIS operating in the S-array configuration.

1.9.4.3 Data and Analysis

Below, we present the the histograms of the distribution D for each of the ten chips. The smooth, solid line is the gaussian fit to D. Each plot also contains the the dark current (ADU/sec) and width[9] (ADU).

[9]Here, the width equals σ, where the gaussian is of the form: $e^{-(x-x_0)/2\sigma^2}$.

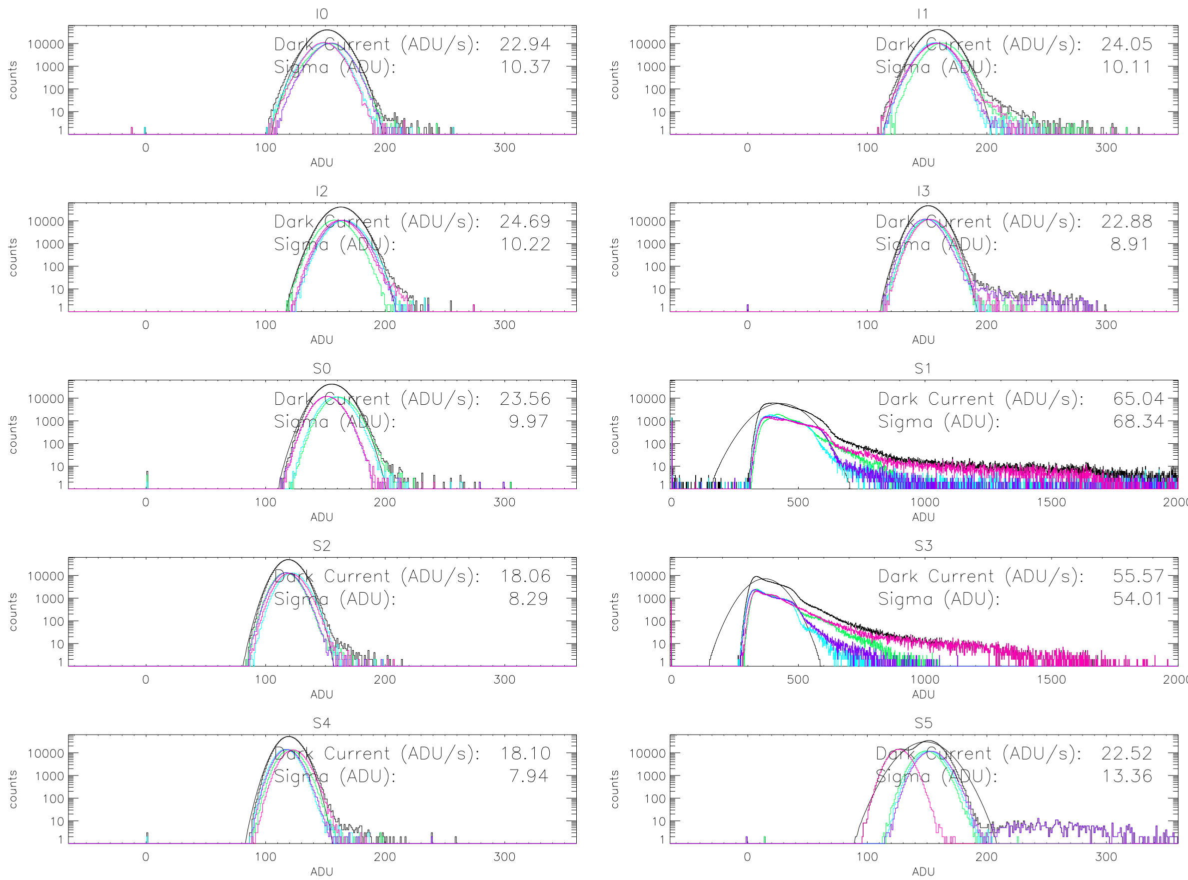

Figure 1.99: ACIS dark current data at T = -40° C.

<u>T = -40° C</u>: Figure 1.99 contains the data for the T = -40° C data. The two backside illuminated (BI) chips (S1 and S3) have a considerable number of hot pixels, as evident by the large, extended tail. The frontside illuminated (FI) chips also have a small number of hot pixels. At this relatively warm temperature, such behavior is expected in both the BI and FI chips.

<u>T = -60° C</u>: Figure 1.100 contains the data for the T = -60° C data. With a drop of 20° C, the dark current in the FI chips is reduced about a factor of 20. The FI chips also have fewer hot pixels at this colder temperature. The dark current in the BI chips is also dramatically reduced. S3 continues to have many hot pixels, and while S1 still exhibits a tail, quadrant by quadrant analysis reveals that most of the tail is attributable to quadrant D (the distribution *D* does not exceed 50 ADU for quadrants A,B, & C).

<u>**T = -90° C**</u>: Figure 1.101 contains the data for the T = -90° C data. At this temperature, the dark current is effectively zero. The difference distributions D are very gaussian, but often have negative centers. These unphysical dark currents arise due to systematic uncertainties, on order of 1 ADU, in calculating the bias. For the relatively short exposure times used and the systematic uncertainties, we cannot precisely measure the *a priori* low dark current (< 0.1 ADU/sec) expected at a temperature of -90° C. With the exception of the hot pixel tail exhibited by S1 and the slightly large width of both S1 and S3, the BI chips are virtually indistinguishable from the FI chips. The secondary feature centered around 9 ADU in I0 is due to a problem with the long (9.9 second) integration data. Examination of the average long frame reveals that the top portion (roughly the first 100 rows) of the bias map is much higher than the rest of the frame. The average short (3.3 second) frame is uniform across the chip. When it is subtracted from the average long frame, the bimodal distribution results. It is suspected that this behavior is due to insufficient settling time between switching ACIS from operation in the the S-array configuration to operation in the I-array configuration.

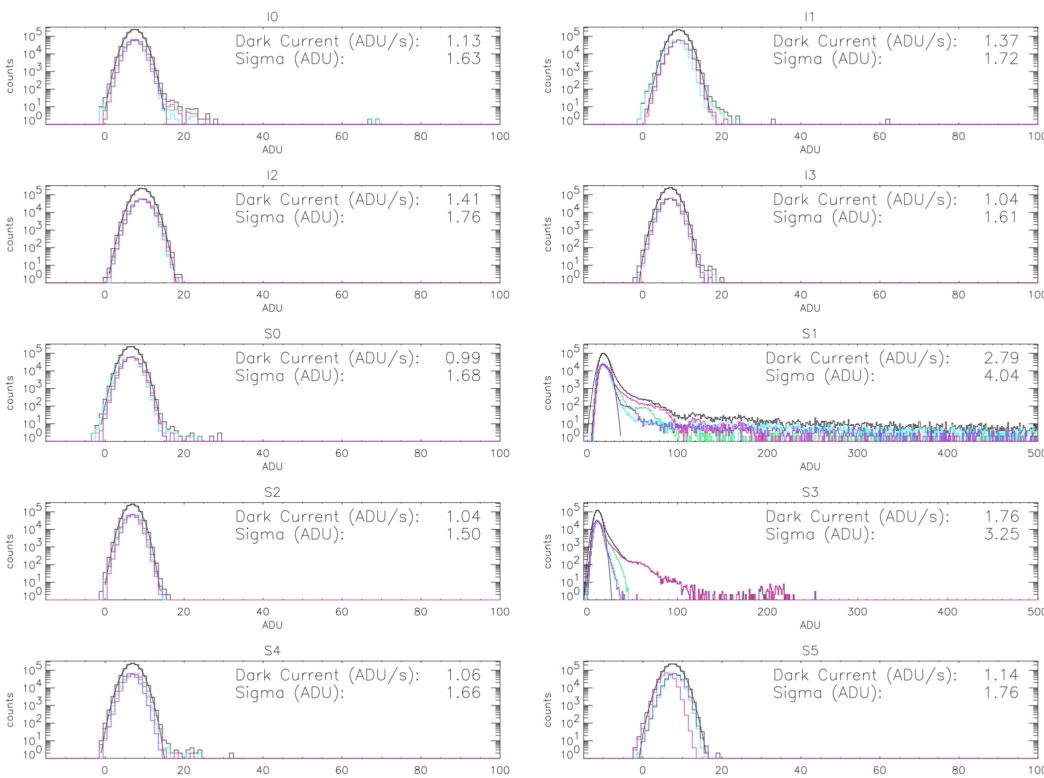

Figure 1.100: ACIS dark current data at T = -60° C.

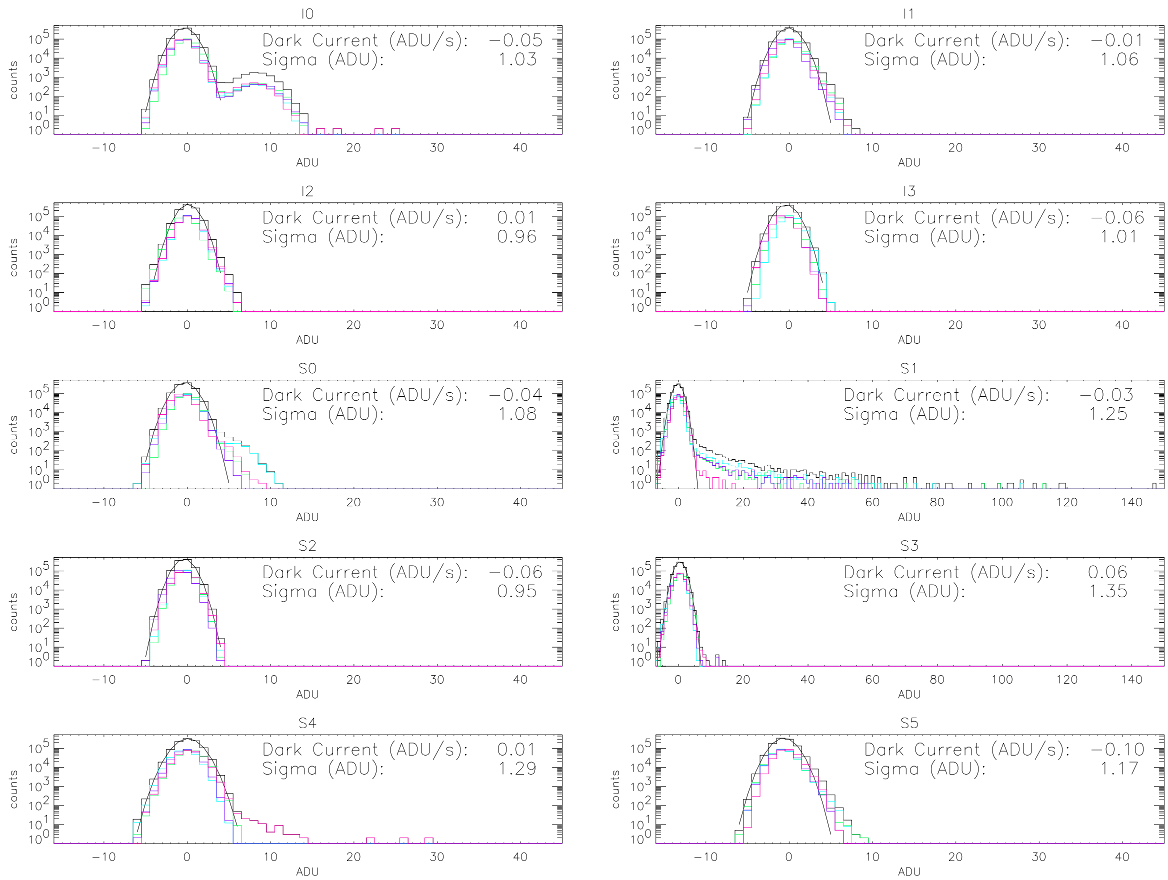

Figure 1.101: ACIS dark current data at T = -90° C.

1.9.4.4 Post Cold Soak Characterizations

One of the procedures performed during the ISIM TV test was to cool the focal plane to T = -129° C. Afterwards, it was important to verify that the cold soak had not damaged ACIS. B. Goeke observed that one way to check for damage to the CCD–to–paddle bond is to measure the dark current. If there is damage, the CCD temperature will rise to the housing temperature (T = -60° C) even if the focal plane is at T = -90° C. Figure 1.102 contains the data taken after the cold soak. The dark current values are entirely consistent with a CCD temperature of T = -90° C, indicating that no damage occured to the bond between the CCDs and the paddle.

1.9.4.5 Summary of Measurements

For future reference, we present the dark current data taken at the ISIM TV test in Table 1.68. Included is the dark current (ADU/sec) and the width (ADU) for each chip.

	T=-40° C		T=-60° C		T=-90° C			
Chip					pre cold soak		post cold soak	
I0	22.9	10.4	1.13	1.63	-0.05	1.03	-0.14	1.13
I1	24.1	10.1	1.37	1.72	-0.01	1.06	-0.07	1.10
I2	24.7	10.2	1.41	1.76	0.01	0.96	-0.02	1.09
I3	22.9	8.9	1.04	1.61	-0.06	1.01	-0.12	1.20
S0	23.6	10.0	0.99	1.68	-0.04	1.08	0.02	1.29
S2	18.1	8.3	1.04	1.50	-0.06	0.95	-0.02	1.29
S4	18.1	7.9	1.06	1.66	0.01	1.29	0.08	1.40
S5	22.5	13.4	1.14	1.76	-0.10	1.17	-0.04	1.21
S1	65.0	68.3	2.79	4.04	-0.03	1.25	-0.06	1.43
S3	55.6	54.0	1.76	3.25	0.06	1.35	-0.08	1.20

Table 1.68: Dark Current Measured at ISIM TV tests during October, 1997. In each column, the number to the left if the dark current (ADU/sec), the number to the right is the width (ADU) of the gaussian fit.

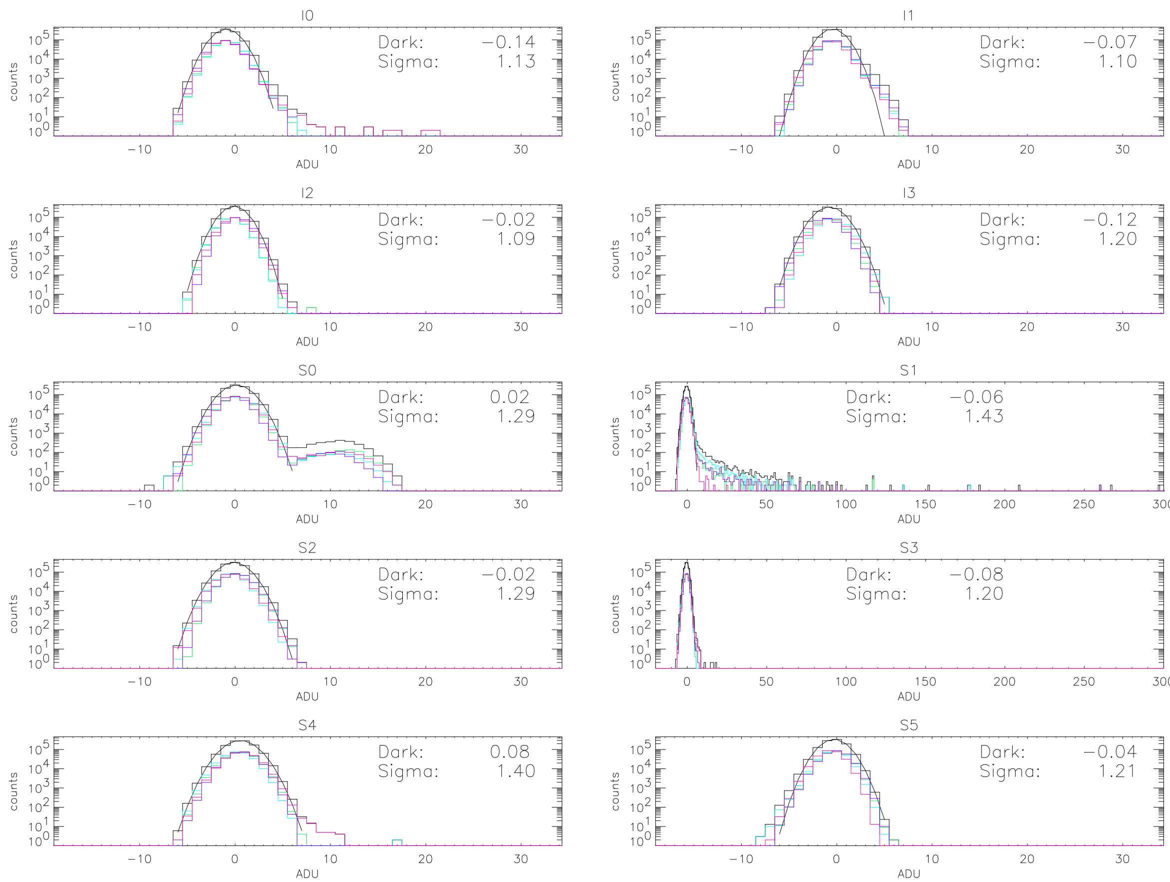

Figure 1.102: Post cold soak ACIS dark current data at T = -90° C.

1.9.5 Effects of CCD Clocking Modes on Detector Peformance

Calibration analyses are based upon data from a timed exposure mode of ccd operation. While this may become the preferred mode of operation it is extremely likely that other operating modes will be used, perhaps even extensively so. Also, most of the analyses, especially of spectral properties such as gain and line shape, are based upon averages of near uniform "flat field" exposures. This type of illumination is not be typical of many sources with the expected telescope point spread function. Illumination and operation mode are closely coupled, the former often dictating the later. Users should consider how operation mode will affect application of the calibration results. For this reason a sampling of representative operating modes was tested and the small differences in performance are now described.

Serial 2 pixel summation reduces the gain by approximately 5 percent owing to the necessary shorter integration pulse widths. Because of the peculiar shape of the integrated waveform the relationship between gain and pulse width cannot be predicted. For example, an adjustable gain feature cannot be reliably invoked via the pulse width - halving the pulse width does not halve the gain (it reduces the gain.) Serial summation also modifies the conventional meaning of event grades by promoting some lower grade events (3 pixel and serial split) into higher grades (single split and single pixel.) The pileup correction will also require modification.

Parallel summation of course alters the conventional meaning of event grades, especially of the parallel split events.

Continuous clocking does not seem to require any special consideration.

The window readout shows a peculiar result worthy of mention. This is a mode wherein a fraction of available rows in a timed exposure are actually clocked through and should not be confused with software window sampling wherein all available rows are clocked through but a software mask excludes events not within a virtual window of rows. For testing purposes a window of 100 rows is used with the result that independent of where the 100 rows occur upon the ccd or what monochromatic x-ray energy is used the measured line widths are always narrower than for the full 1024 row readout. Typically the differences is no more than 5 percent. The cause of this change in line width remains a mystery. A leading candidate is the "Elvis-effect", a multilevel disturbance in the bias level which occurs and endures for times comparable to the 100 row readout time. The cause of the Elvis-effect is unknown and it is unclear if it occurs with the flight configured instrument. This is one of a class of bias distortions which would not affect spectra from spatially localised events, but would impact spectra from flat field type illuminations.

The effects of various operating modes are small and occur through the electronics or the meaning of event grades, gain, noise, etc. The description of the ccd model is not affected by choice of operating mode.