An ASIC for Delta Sigma Digitization of Technical CCD Video

John P. Doty[a], D. Matsuura[b], H. Ozawa[b], E. Miyata[b], H. Tsunemi[b] and H. Ikeda[c]

[a]Noqsi Aerospace Ltd., 2822 S. Nova Rd., Pine, Colorado, USA;
[b]Graduate School of Science, Earth and Space Science Osaka University, Machikaneyama, 1-1 Toyonaka, Osaka, 560-0043, Japan;
[c]Japan Aerospace Exploration Agency (JAXA) / Institute of Space and Astronautical Science (ISAS), 3-1-1 Yoshinodai, Sagamihara, Kanagawa, 229-8510, Japan

ABSTRACT

Delta Sigma digitizers generally have excellent linearity, precision and noise rejection. They are especially well suited for implementation as integrated circuits. However, they are rarely used for time bounded signals like CCD pixels. We are developing a CCD video digitizer chip incorporating a novel variant of the Delta Sigma architecture that is especially well suited for this application. This architecture allows us to incorporate video filtering and correlated double sampling into the digitizer itself, eliminating the complex analog video processing usually needed before digitization.

We will present details of a multichannel ASIC design that will achieve spectroscopic precision and linearity while using much less energy than previous CCD digitizers for technical applications such as imaging X-ray spectroscopy. The low conversion energy requirement together with the ability to integrate many channels will enable us to construct fast CCD systems that require no cooling and can handle a much wider range of X-ray intensity than existing X-ray CCD systems.

Keywords: Charge Coupled Device, CCD, Delta Sigma, ADC

1. INTRODUCTION

The "differential averaging" function (Fig. 1 left) is optimal for measuring CCD video from the usual floating diffusion output in the presence of "kTC" and white noise, and is near optimal for removing $1/f$ noise as well.[1] In a system using this approach, circuitry computes an approximation to the integral of the product of video voltage with this function to obtain a pixel value. This computation is usually performed in the analog domain.

Similarly, a delta-sigma analog-to-digital converter[2] integrates the product of the signal with a sampling ("decimation") function.[3] However, a suitable function (Fig. 1 right) is very different from the differential averaging function. In this case, the computation is performed in the digital domain. This simplifies the analog part of a measurement system considerable, and the analog part is usually relatively bulky and inefficient. This,

Further author information: (Send correspondence to J.P.D.)
J.P.D.: E-mail: jpd@wispertel.net, Telephone: +1 303 816 2756
D. M.: E-mail: matsuura@ess.sci.osaka-u.ac.jp, Telelephone: +81-6-6850-5475
H. O.: E-mail: ozawa@ess.sci.osaka-u.ac.jp, Telephone: +81-6-6850-5476
E. M.: E-mail: miyata@ess.sci.osaka-u.ac.jp, Telephone: +81-6-6850-5475
H. T.: E-mail: tsunemi@ess.sci.osaka-u.ac.jp,Telephone: 81-6-6850-5477
H. I.: E-mail: ikeda.hirokazu@jaxa.jp, Telephone: +81-42-759-8362

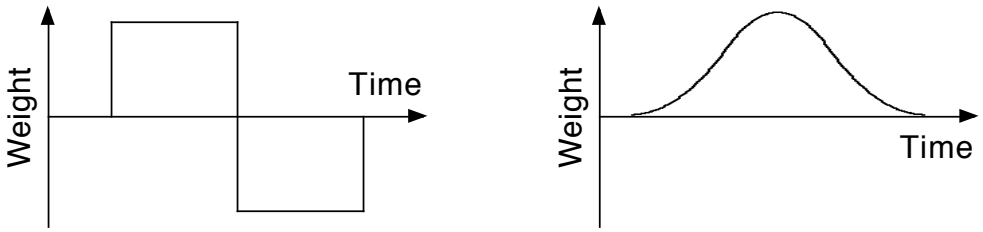

Figure 1. Sampling functions for computing a weighted average signal. Left: differential averaging function, optimal for removing thermal noise from CCD video. Right: decimation function, optimal for removing digitization noise from delta-sigma modulator output.

along with the linearity and accuracy advantages of the delta-sigma technique, has made this the technique of choice in most applications (especially audio and measurement) where the decimation filter characteristics are compatible with other application requirements.

We believe that CCD imaging systems could benefit from the advantages of the delta-sigma technique. Since a complete delta-sigma digitizer can be implemented in mixed-signal VLSI, systems with large numbers of channels may be assembled. Reading out many video channels in parallel allows rapid readout while keeping the bandwidth of each individual channel low for low noise. Moving most of the signal processing from bulky, power-hungry analog circuitry to compact, efficient digital circuitry is helpful in many applications. Users of nondispersive x-ray spectroscopy systems frequently request very high differential linearity to facilitate line profile studies below the spectrometer resolution at high signal to noise: delta-sigma digitizers generally have extremely good differential linearity.

The incompatibility of the differential averaging function with an effective delta-sigma decimation function has inhibited the application of this promising technique to CCD video. The differential averaging function has sharp edges to optimally reject low frequency noise present in CCD video, and to keep signals from separate pixels separated. On the other hand, a delta-sigma decimation function needs to be very smooth to reject high frequency noise generated by the delta-sigma converter itself.

2. CONCEPT

A conventional delta-sigma digitizer has the structure in Fig. 2. The modulator converts the input signal into a sequence of low precision (often just one bit) digital numbers whose average represents the level at the analog input. Because these numbers are of low precision, the level of "digitization noise" in the modulator is high. The digital filter removes most of this noise, recovering a precise digital representation of the input by computing a weighted average of the low precision numbers from the modulator. The modulator design facilitates this by "noise shaping":[3] the noise in the modulator output is concentrated at high frequencies, so a low pass filter can effectively remove most of it.

By preceding a conventional delta-sigma converter by a "premodulator" that multiplies the incoming video signal by the differential averaging function (Fig. 3), we obtain a video processor[4] with a sampling function approximating the optimum. The resulting video processor would operate in four phases as shown in Fig. 4 . During the "Pre" phase, the modulator processes zero signal from the modulator. During the "Deint" phase, the modulator processes positive signal representing the video baseline. During the "Int" phase the modulator processes inverted video signal: since the video from an N-channel CCD is negative, this produces a positive response to illumination. Finally, during the "Post" phase the modulator again processes zero signal from the premodulator.

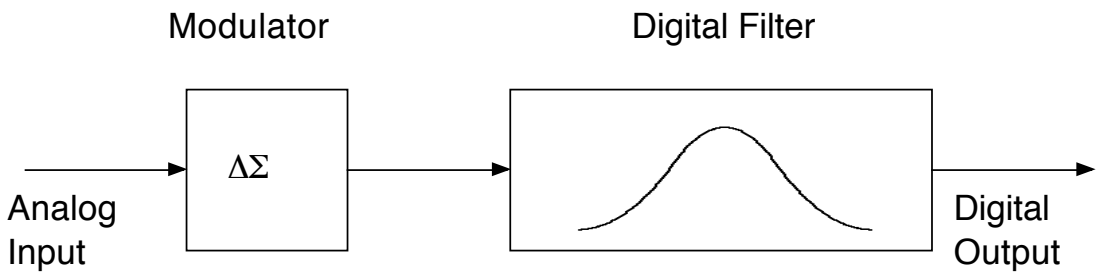

Figure 2. A conventional delta-sigma digitizer.

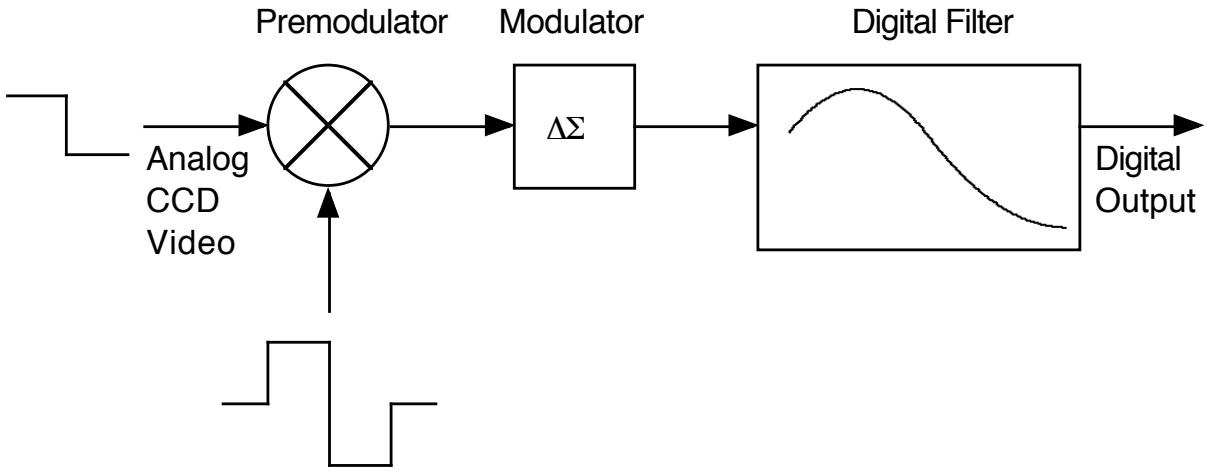

Figure 3. Adding a premodulator to the delta-sigma digitizer allows it to approximate the differential averaging function for video filtering, while still using an effective digital decimation filter function.

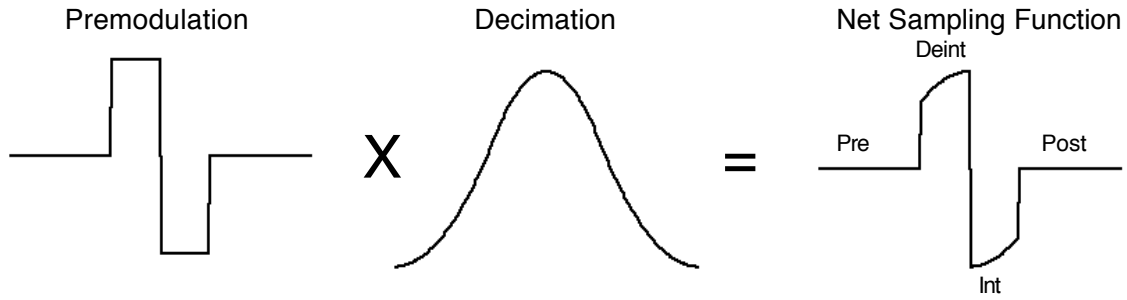

Figure 4. The combined effect of premodulation and decimation.

The sampling function of the decimation filter is still smooth, so it remains effective at removing modulator noise. Since the premodulator is ahead of the modulator, it has no effect on the modulator noise the decimation filter is designed to remove, but it changes the overall system sampling function to a form nearly optimum for CCD video.

We can simplify this by eliminating the "Pre" phase. Assuming that the modulator is in a known state at the start of this phase, the resulting output is, in the ideal case, perfectly predictable. Therefore, we can initialize the modulator to a known state just before starting the "Deint" phase without loss of information. This eliminates one of the wings of decimation filter's sampling function, but since the incoming video would have no influence on the modulator during this phase, the result of the resulting sharp edge is not noise but simply a small fixed offset. Since in a practical CCD system other (generally larger) offsets must be removed by calibration and subtraction anyway, this is not a problem.

Unlike the "Pre" phase, the "Post" phase cannot be eliminated. At the start of this phase the modulator is in an unknown state, as it has been responding to video input. Thus, a sharp edge in the decimation filter's sampling function would allow unevaluated modulator noise into the result.

3. IMPLEMENTATION

We have designed a four channel CCD measurement chain chip, designated "MD01", using this approach. The design is intended for the TSMC 350nm mixed signal CMOS process. We have designed analog subcircuits like amplifiers, comparators, and charge pumps especially for this chip. We have adopted OpenIP[5] designs for digital and interface subcircuits where applicable.

Fig. 5 shows the (conceptual) architecture of a delta-sigma modulator within the MD01 chip. A switched capacitor approach is relatively easy to analyze, and allows the clock rate to vary without major gain shifts up to the maximum rate the technology can support. Charge pumps convert voltage to charge, and integrators sum charge and convert it back to voltage. Two integrators make this a "second order" modulator.

It is easy to disable or change the sign of the voltage to charge conversion in a charge pump, so the INPUT charge pump also acts as the premodulator. $VREF$ represents the saturation level of the modulator: for good linearity the nominal $VIDEO$ input range is $\pm 0.5\ VREF$.

The SHAPING charge pump with its integrator increases the modulator's low frequency feedback for noise shaping.[3] The ERROR SUM capacitors combine the first and second order error signals, feeding the comparator/flip flop combination that generates the output and controls the polarity of the FEEDBACK charge pump. The $CLAMP$ signal reinitializes the modulator between conversions.

Simulations (section 3.1) show that the 4:1 ratio of integration capacitance to pump capacitance yields optimum noise shaping and is also a good choice for dynamic range control. The actual MD01 modulator design is fully differential for easier implementation with a single power supply and better rejection of external noise.

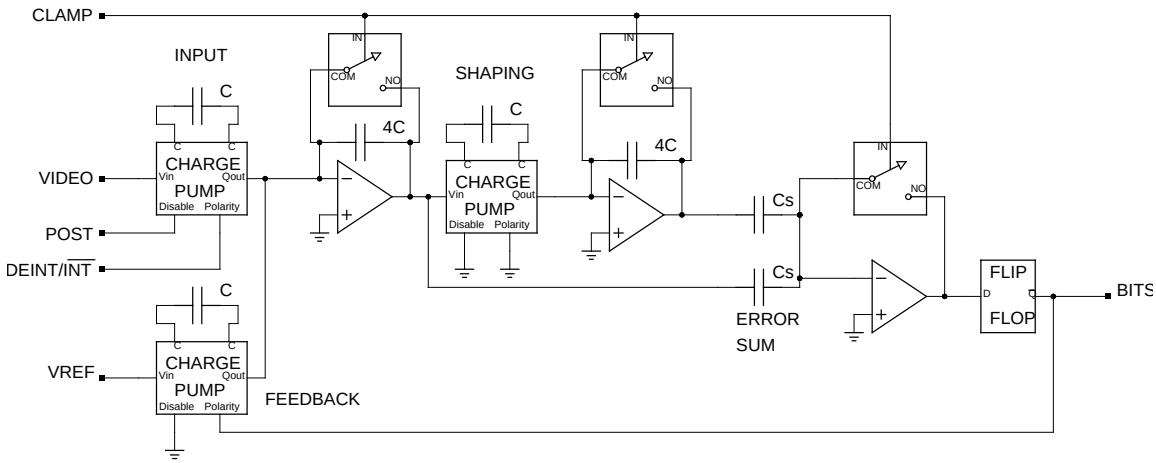

Figure 5. Conceptual architecture of the delta-sigma modulators within the MD01 chip. Clocks are not shown.

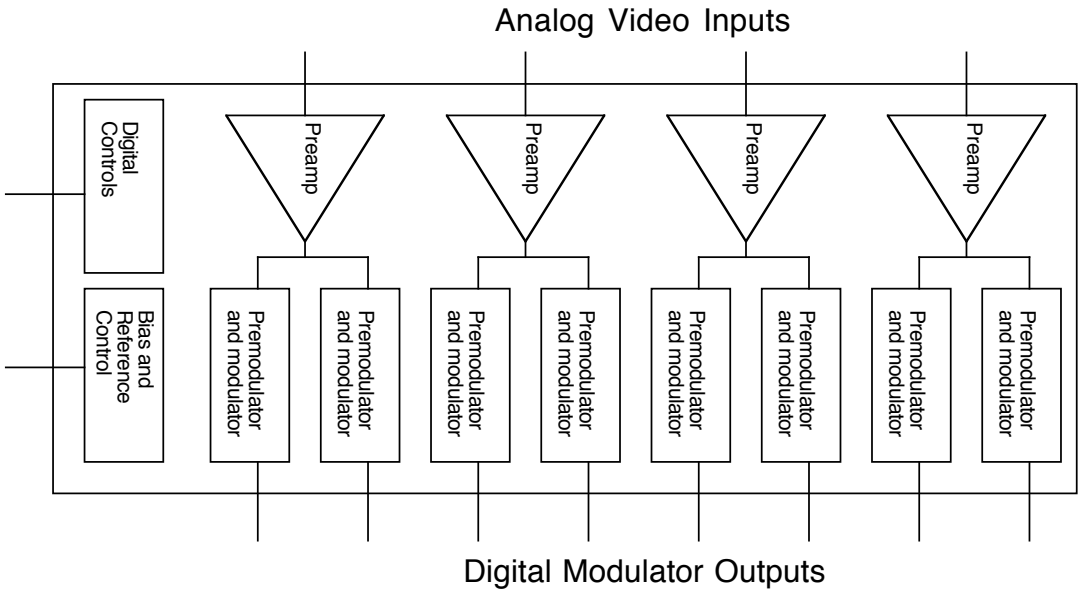

Figure 6. Block diagram of the MD01 chip.

A low noise preamplifier with a gain of ~ -10 feeds the VIDEO input. The preamplifier incorporates a digital to analog converter whose output is subtracted from the signal during the "Int" phase: this allows a rough correction of video bias. The preamplifier is also a fully differential circuit, with inputs clamped between pixels to allow capacitive coupling from the CCD. The inputs can thus accommodate any DC output level and polarity.

Each preamplifier feeds two modulators. The modulators alternate: one processes even numbered pixels while the other processes odd numbered pixels. This allows adequate time for the "Post" phase of modulator

operation without requiring the CCD readout to pause between pixels. Oversampling rates of up to 100 MHz are possible. We expect this to yield about 12 bits of useful precision at a pixel rate of 1 MHz. There is no decimation filter in the MD01, so outputs are bit streams at the oversampling rate. These outputs use "low voltage differential signaling" (LVDS) standards to minimize crosstalk with analog circuitry. External signals also control the timing of the phases of converter operation: these signals along with the oversampling clock input also use LVDS. Standard low voltage CMOS inputs provide power-on reset capability and the ability to serially load the video bias digital to analog converters.

Fig. 6 shows the top level architecture of the MD01. With its timing and decimation handled externally, the MD01 may be applied to a variety of CCD systems. We can control the oversampling rate and the number of samples per pixel to adjust pixel rate and dynamic range. We can optimize the decimation filter for the noise characteristics of the video signal.

We have sent the MD01 schematic design to Digian Technology for layout. We expect a draft layout at the end of May, 2006.

3.1. SIMULATIONS

We have performed two kinds of simulations for the MD01 chip. First, we used an abstract modulator simulation to explore modulator architecture and optimization. Second, we used circuit simulations to test and verify the detailed circuit design, from the subcircuit level up to the whole chip level. The abstract modulator simulation can simulate about 1 million pixel conversions per hour. The circuit simulation is about 100,000 times slower.

The abstract modulator simulation treats the modulator as an iterated function system using Mathematica. We can inspect phase space trajectories of the modulator as diagnostics and to determine the required internal dynamic range for circuit design. We can experiment with different architectures. We can apply either noiseless or noisy inputs. We can determine optimum decimation filter sampling function by least-squares fitting.

The modulator architecture in Fig. 5 was the result of these simulations. With "Deint" and "Int" phases of 32 oversamples each, and a "Post" phase of 96 oversamples, an optimal decimation filter yields residual RMS digitization noise of $\sim 1/3000$ of the nominal signal range. In these simulations, differential and integral nonlinearity are undetectable.

Fig. 7 shows a simulation of the conversion of a single pixel. The pixel rate is 1 Mpix/s, the oversampling clock is 96 MHz. The curve in (a) starts with a 50 mV video reset pulse from the CCD, followed by video baseline. The preamplifier input is AC coupled: a clamp in the preamplifier pulls the video baseline to zero immediately after the reset pulse. The clamp is then released to allow the modulator to integrate the residual baseline level: this yields better kTC noise rejection than the clamp alone.

After the video baseline, the 35 mV downward step represents charge clocked into the CCD output stage. The preamplifier subtracts a programmable level, -30 mV in this simulation, from this step to approximately cancel the video bias. The preamplifier amplifies the result by -10, yielding (b). This simulation includes noise from the CCD, easily seen in the preamplifier output here.

The input charge pump yields (c). Each point represents a charge packet: the units are femtocoulombs. The noise shaping filter produces (d) from the filtered difference of the charge from the input and feedback pumps. This drives the comparator, yielding bit stream (e), which controls the sign of 24 fC packets pumped by the feedback pump, and also feeds the external decimation filter.

The decimation filter computes the conversion result as a weighted sum of the bits in (e). (f) shows the product of the bits with the weights, normalized so that the average is the desired result. In this case, the result is 5.05 mV, slightly higher (because of the simulated noise) than the expected 5 mV. Note that this is small compared to the thrashing in (f): the decimation filter is very effective!

We have used ngspice[6] for most of our circuit simulations. For the high level simulations a stimulus generator in a simplified Forth dialect produces the input signal descriptions. A pipeline of simple C programs reduces the output to bits and then applies the optimum decimation filter from the abstract modulator simulation above. The results are similar to the results of the abstract simulation, but neither as extensive nor as precise. The

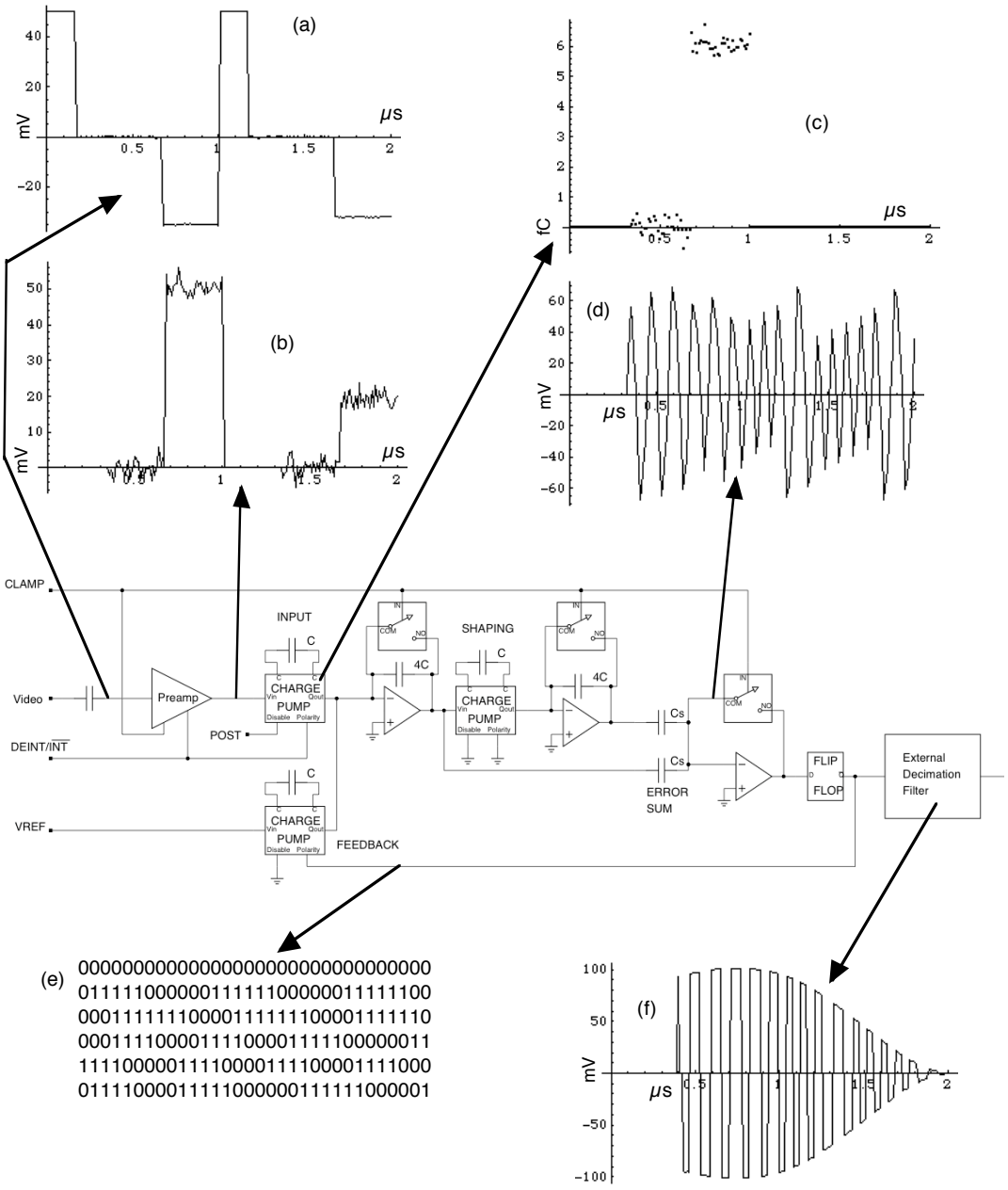

Figure 7. Simulation of MD01 architecture. (a) is video input.The preamplifier amplifies, gates, and removes bias, yielding (b). The modulator input pump converts the signal to charge, switching signs at the transition from video baseline to video signal, and selects the first pixel of the pair, yielding (c). The second order shaping filter processes the difference between the signal charge and the feedback charge, yielding (d). From (d), the comparator extracts the sign of the filtered error signal, yielding serial digital output (e), which also drives the feedback pump. The decimation filter weights the serial output: the average of (f) is the converted result.

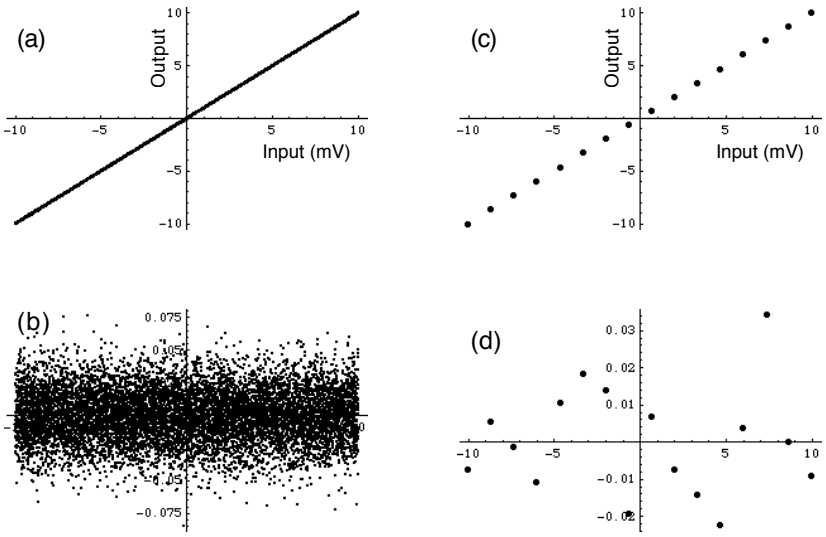

Figure 8. Linearity and accuracy of the MD01 from simulations. 10,000 runs of a simulation in Mathematica similar to that in Fig. 7 yielded (a). The x-axis is input in mV following bias subtraction and the y-axis is the resulting converter output after calibration. (b) shows the residual errors in mV. (c) is from a circuit simulation with ngspice, and (d) shows the residual errors from that simulation.

numerical dynamic range of SPICE is not adequate to verify the performance of this complex circuit at a level below $\sim 0.1\%$.

Fig. 8 shows studies of linearity and accuracy using both simulation methods. The lower plots, (b) and (d) represent residual conversion errors from the points in the upper plots, (a) and (c). The scatter in (b) is mainly due to simulated noise in the video, while the simulation in (d) included no noise. The scatter in (d) is apparently due to numerical calculation errors in SPICE: the magnitude of this scatter is sensitive to parameters of the SPICE simulator itself. Neither simulation shows significant nonlinearity.

When the layout parasitics have been determined, we will perform additional SPICE simulations to verify the equivalence of the silicon level and schematic level designs.

3.2. EXPECTED PERFORMANCE

The following are estimates based on the simulations, supplemented by pencil and paper calculations. We expect that the dominant noise source will be $1/f$ noise in the preamplifiers, so noise should not be a strong function of pixel rate. At the nominal maximum 1 MHz pixel rate, kTC noise from the charge pumps approaches the preamplifier noise, and digitization noise is also a factor. Although operation at higher rates is possible, performance will decline very rapidly as the rate is increased. The nominal video full scale voltage is 20 mV.

Channels: 4

Power consumption: 60 mW

Noise: 18μV RMS

Maximum removable video bias: 70 mV

Integral Nonlinearity: $< 0.1\%$

Differential Nonlinearity: $< 0.01\%$

4. FUTURE WORK

We expect to have prototype chips in hand by the fall of 2006. We will characterize these at Noqsi Aerospace and Osaka University. Once we are satisfied that they are working properly, we will try these in a CCD system at Osaka University.

For a next generation chip, we intend to put the decimation filter and control logic on the chip, reducing support requirements and simplifying interfaces. This should also make a chip with more channels practical.

ACKNOWLEDGMENTS

The work described above would have been impossible without good electronic design automation (EDA) tools, For a part-time designer working on a moderate-budget project, commercial EDA tools are extremely expensive. They are also complex and difficult to learn. Fortunately, there is now a practical alternative. This project used free open source tools for EDA: "gEDA" for schematic capture and netlist generation,[7] "ngspice" for simulation,[6] and "spicepp" for fixing SPICE dialect incompatibilities.[8] We would like to thank all the developers of these tools, especially Ales Hvezda (gEDA project leader), Stuart Brorson (for SPICE support, excellent documentation and a timely bug fix), and Dan McMahill (for helpful advice).

This work is partly supported by a Grant-in-Aid for Scientific Research by the Ministry of Education, Culture, Sports, Science and Technology of Japan (16002004).

Matthew Wampler-Doty assisted the preparation of this manuscript.

REFERENCES

1. D. J. Hegyi and A. Burrows, "Optimum sampling of charge-coupled devices," *Astron. J.* **85**, pp. 1421–1424, 1980.
2. H. Inose, Y. Yasuda, and J. Murakami, "A telemetering system by code modulation, delta-sigma modulation," *IRE Trans. on Space Electronics and Telemetry* **SET-8**, pp. 204–209, 1962.
3. S. Park, "Principles of sigma-delta modulation for analog-to-digital converters," tech. rep., Motorola Literature Number APR8/D.
4. J. P. Doty. US patent application serial number 11/307435, international serial number PCT/US2006/004330, 2006.
5. http://research.kek.jp/people/ikeda/openIP/.
6. http://ngspice.sourceforge.net/.
7. http://geda.seul.org/.
8. http://tclspice.sourceforge.net/.